The Gemini MultiBoard Microsystem

FDC/SASI

80-BUS
Floppy Disk SASI Controller Board
Instruction Manual
&
Functional Specification

GM 829
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Introduction

The Gemini GM829 is an 80-BUS and Nasbus compatible combined Floppy Disk Controller (FDC) and Shugart Associates Systems Interface (SASI) board for use with Gemini MultiBoard and Nascom systems. The board has been designed to allow it to be used with up to four mixed 5.25" and 8" drives. These may be single or double sided, ordinary or double track density drives, in single or double density formats. Switching between single and double density, and between 5.25" and 8" drives, is under software control. The board also has variable write precompensation and phase locked loop data recovery circuitry. The controller I.C. used is the Western Digital 1797.

In addition to floppy disk drive support the GM829 board offers a SASI interface for the connection of a hard disk (Winchester) drive sub-system. The Gemini GM835 series has been designed to plug directly into the GM829's SASI socket.

The GM829 board occupies a group of 8 x Z80 I/O ports, and these ports may be located in one of two positions, allowing up to two boards to be used in a single system. When used with 5.25" drives this board is completely software compatible with the earlier Gemini GM809 board.

Commissioning

Carefully unpack your GM829 and examine it for any mechanical damage. In the event of any damage please inform your dealer immediately.

Your GM829 will have been shipped to you fully tested and working. Dependant on the type of disk drives being used all that may be required is for the board to be plugged in. However, please take time to read through this manual as it may prove useful.

When plugging the GM829 into the bus, please take care. Excessive force should not be required. Any difficulty which may be encountered will, in all probability, be due to the keyway of the edge connector not fitting accurately into the slot in the edge of the board. Please ensure that the board is plugged in with the edge connector going in first and the correct way round. It is not possible to plug the board in the incorrect way because of the keyway.

The floppy disk drives are connected to the GM829 via the 34 way (PL2, for 5.25" drives) and 50 way (PL3, for 8" drives) connectors on the board, and the SASI hard disk sub-system via the second 50 way (PL1) connector. The pin 1 end of each connector on the board is identified by a '1' on the PCB and an arrow head or other marking on the connector itself. Ensure that the cable is connected with the correct orientation, or damage may occur to the board and drives.

There are several linking options on the GM829. These have been set during manufacture and full details are provided in the section on links, to allow the user to configure the board to his own requirements.

Links.

There are seven linking options on GM829. All link options are set at manufacture by PCB tracks. However, if alternative settings are required, then the PCB tracks linking the pads should be cut and new links should be made by soldering wire from one pad to the other. Please take great care as an incorrect link may cause damage and a poor connection will result in an unreliable system.

Link 1. (LK1). 5.25" Drive type.

There are two alternative 'standards' for the pin out of the 34 way connector (PL2) for 5.25" drives and the LK1 link block is used to select between them. LK1 is placed above IC3.

If pin 6 of the drive connector is the fourth drive select line (ISLT3), then B should be linked to C. Alternatively if pin 34 of the drive connector is the fourth drive select line (DS4), then C should be connected to D. In the latter case pin 6 will be the drive ready line (RDY), and so B and A should also be connected.

For example: Pertec FD 250 drives - link B to C
Micropolis 1015 drives - link A to B, and C to D *

Also see link 3.

Link 2. (LK2). 1797 clock.

This link is used to provide the necessary clock to the 1797 FDC chip via a software controlled 'divide by 2' stage.

LK2 is placed between IC6 and IC11. A 2 MHz clock, derived from the 80-BUS system clock, is required at point B. At point C is the system clock itself, and at point A the system clock divided by two. This link therefore should be set as follows:

A - B for 4 MHz CPU clock *
C - B for 2 MHz CPU clock

For systems with different CPU clock speeds, see link 6 below.

Link 3. (LK3). Ready line connection.

This link should be inserted when pin 6 of the drive connector is the ready line (RDY), or if 8" drives are being used. This link is placed between IC7 and IC8 and should be present for Micropolis 1015 type drives and 8" drives.

linked *

* links as supplied.

Link 4. (LK4). Write Precompensation selection.

This link area is used to enable/disable the write precompensation circuitry. Different options may be selected for both 5.25" and 8" drives. Each of these may be set to disable the write precompensation circuitry, although this would only normally be done to test the board.

Alternatively write precompensation may be provided on all tracks, or only on tracks beyond track 43 on either drive. This latter option should normally be chosen for 8" drives, and for 5.25" drives with more than 40 tracks per side.

LK4 is positioned below IC7, and link options are shown below. (Note: NC=no connection.) The write precompensation circuitry is only enabled when the system software selects double density operation.

	5.25" drive	8" drive
No write precomp.	D-C	B-C
Write precomp. track 43+	D-A *	B-A *
Write precomp. all tracks	NC to D	NC to B

Link 5. (LK5). Z80 Port addresses.

This link selects one of the two blocks of Z80 port addresses that this board may occupy. LK5 is positioned below IC23. Linking A to C locates the board at Ports C0-C7, linking A to B locates the board at ports E0-E7. The latter is the normal configuration.

A-B *

Link 6. (LK6). Clock selection.

This link determines the source of the clock on the GM829, and is positioned below IC26. If B is linked to C, the clock will be taken from the bus AUXCLK line. If B is linked to A, the clock will be taken from the main system clock line, and this is the normal position. If the host system is running at 2 or 4 MHz, then the clock signal required by the 1797 FDC can be provided by appropriate selection at link 2. However, if a different system clock is used, then a 4 MHz clock should be provided on the AUXCLK bus line, and B should be linked to C. For full details of implementing the AUXCLK line, please see the manual for the bus master.

A-B *

Link 7. (LK7). SASI line 32 select.

Link 7 is used for SASI devices requiring the /ATN signal on line 32 of the interface. LK7 is located on the GM829 above IC2. The signal is present if the link is fitted. It is not required for the Gemini GM835 hard disk sub-systems.

No link *

Connectors.
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The GM829 is provided with a 34 way insulation displacement connector (PL2). This is the standard type of connector used with 5.25" drives. It is also fitted with two 50 way insulation displacement connectors, PL1 and PL3. PL3 is the standard type of connector used with 8" drives, and PL1 is that used by SASI devices. The pin 1 end of each connector on the board is identified by a '1' on the PCB and an arrow head or other marking on the connector itself. Ensure that the cable is connected with the correct orientation, or damage may occur to the board and drives.

Potentiometers.

There are 3 multiturn potentiometers on GM829. These have been set at manufacture for 5.25" drives and 250 nS write precompensation. If alternative adjustments are required, these should be made with reference to a 1797 data sheet and the GM829 circuit diagrams. DO NOT adjust the potentiometers unless the board is to be used with alternative drives as this may negate any warranty claim.

VR3 is set (while no data is being transferred) for 1.45V +/- 0.05V at Pin 2 of the 74LS629 VCO (IC 13) (TP5).

VR1 is adjusted to provide a 4 MHz (+0% -5%) clock signal at Pin 7 of the 74LS629 VCO (IC 13), or a 2 MHz (+0% -5%) clock signal on TP2, provided the GM829 is software selected to 5.25" operation.

VR2 is used to set the required write precompensation timing (Nominally 250nS). It should be adjusted whilst formatting in double density for the desired effect at Pin 6 of the WD 1691 FSL (IC 17)(TP1). Trigger a 'scope from IC17 pin 1 (TP3) and adjust the delay between the start of the 'early' and 'late' pulses to twice the desired precompensation value.

Notes on 8" operation.

Bit 5 of the floppy control port (Port C4 or E4) is used to control the switching of a number of signals on the GM829. These correspond to the differences normally necessary to switch operation between 5.25" and 8" drives, and all references in this manual correspond to these. However, there may be occasions when it is useful to switch these signals for alternative purposes, and the following information may prove useful.

Bit 5 Port C4/E4	0	1
1797 clock =	1 MHz	2 MHz
1691 VCO =	2 MHz	4 MHz
1797 READY line generated by -	Motor-on AND Head loaded AND Drive RDY	Drive Ready ONLY
Write Precomp. determined by -	Connection to 'a' on LK4 (see above)	Connection to 'b' on LK4 (see above)

Note that it is possible to write code to service the 1797 controller in seven of the permutations of:

5.25" or 8" drives
single or double density modes
Z80 CPU clock of 2 or 4 MHz

The illegal permutation is to use 8" drives in double density mode if the Z80 CPU is only running at 2 MHz.

Nascom 2 Modification

In the Nasbus specification the bus reset pulse (line 14) was specified as 10 uS. In the 80-BUS specification this has been extended to 50 uS, as chips in the 179X family require a reset pulse of this duration. In practise this has not been found to cause a problem. However, Nascom 2 owners using the GM829 who are concerned by this should substitute a 10 nF capacitor for C1 (previously 1nF) on their Nascom 2.

Preferred Drives.

The GM829 design has been tested for use with the following drives in both single and double density modes:

Shugart SA200	-	5.25", single sided, 48 TPI, 40 track
Pertec FD250	-	5.25", double sided, 48 TPI, 35 track
Teac FD-55E/55F	-	5.25", single/double sided, 96 TPI, 80 track
Micropolis 1015F5/F6	-	5.25", single/double sided, 96 TPI, 80 track
Pertec FD650	-	8", double sided
Shugart SA800/850	-	8", single/double sided
Tandon TM848-1/-2	-	8", single/double sided

The Micropolis drives are the recommended drives for use with the board, and software support is currently based on these. Alternative drives may be used, but it must be pointed out that although other drives may be electrically compatible, there are often small differences in timing that would require modification to any software written specifically for the above drives.

CP/M 2.2 is available configured for use with GM829 and Pertec FD250 or Micropolis 1015 drives for:
(a) Nascom 1 or 2 with Nascom screen or Gemini GM812 IVC board (80x25).
(b) Gemini MultiBoard System (GM811 CPU or GM813 CPU/RAM).

For Nascom owners Polydos is available as an alternative operating system to CP/M for use with the GM829 and Pertec FD250 or Micropolis 1015 drives.

Software for other drive types may become available and any Gemini dealer should be able to keep you informed of further developments.

Drive Address Selection

Up to four floppy disk drives may be connected to the GM829, and these may be either 5.25", 8", or a combination of both. Note that all drives of the same size should be of the same type. The 34 and 50 way floppy drive connectors (PL2 & 3) are basically connected in parallel, and so should be considered as being on the same connector as regards selecting drive addresses.

GM829 Specification

1. Electrically and physically compatible with 80-BUS and Nasbus.

2. Operates with 5.25" and 8" drives.

3. Operates up to four drives. Drives of each size (5.25" and 8") must be of the same type.

4. Operates with single or double density, single or double sided drives.

5. Operates with 2 MHz or 4 MHz CPU clock. (Software timing may be critical.)

6. Continuously variable write precompensation in double density mode.

7. Single/double density selection under software control.

8. 5.25"/8" selection under software control.

9. Phase locked loop data recovery circuitry.

10. Utilises Western Digital FD1797 controller.

11. Incorporates hardware delays (a) Head load - 45 mS nominal.
(b) Motor on - 1 sec.nominal.

12. Motor time out approximately 10 seconds after last write to drive select latch.

13. Two boards may be used in the same system, allowing up to 8 floppy drives.

14. The board may occupy Z80 read/write ports C0H-C7H or E0H-E7H (i.e. 8 ports) thus:

C0-C3	or	E0-E3	: 1797 controller
C4	or	E4	: Write - drive and density select
			Read - flag read
C5	or	E5	: Write - SASI control
			Read - SASI status
C6	or	E6	: SASI data
C7	or	E7	: Decoded but unused

15. Port C4/E4

Bits	Write	Read
0	Select drive 0	INTRQ from 1797
1	" " 1	NOT READY *
2	" " 2	0V
3	" " 3	0V
4	Select density	0V
5	Select 5.25"/8"	0V
6	Not used	0V
7	Not used	DRQ from 1797

Connector Details

PL1 - 50-way Connector

Line Number	SASI Signal
2	Data 0
4	Data 1
6	Data 2
8	Data 3
10	Data 4
12	Data 5
14	Data 6
16	Data 7
32	/ATN
36	/BUSY
38	/ACK
40	/RST
42	/MSG
44	/SEL
46	C/D
48	/REQ
50	I/O

All odd pins (1-49) are grounded.
Line 34 is implemented by inserting LK7

PL2 - 34-way Connector

Line Number	Pertec FD250 signal	Micropolis 1015 signal	GM829 implementation
6	ISLT3	/RDY	* Drive select D/Ready line
8	IINXP	/SECP	Index Pulse
10	ISTLO	/DS1	)
12	ISTL1	/DS2	)Drive select lines A-C
14	ISLT2	/DS3	)
16	IDEN	/MTRN	Drive motor enable
18	IDIR	/DIRN	Direction select
20	ISTP	/STEP	Step
22	IWDA	/WDA	Write data
24	IWGT	/WRT	Write gate
26	ITRKO	/TRKO	Track 0
28	IWPT	/WPT	Write protect
30	IRDA	/RDA	Read data
32	ISSLT	/HSLT	Side select
34	Spare	/DS4	* Unused/Drive select D

All odd pins (1-33) are grounded.
* The function of lines 6 & 34 are selected by link 1.

PL3 - 50-way connector

Line Number	Pertec FD650 signal	GM829 implementation
2	IHCS	Head current switch
14	ISSLT	Side select
20	IINXP	Index pulse
22	IDRDY	Drive ready
26	ISLT0	)
28	ISLT1	)Drive select lines
30	ISLT2	)
32	ISLT3	)
34	IDIR	Direction select
36	ISTP	Step
38	IWDA	Composite write data
40	IWGT	Write gate
42	ITRK0	Track 0
44	IWPTD	Write protect
48	IRDA	Composite read data

All odd pins (1-49) are grounded.

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